Context and motivation

In the upcoming era of Mobile, IoT, CPS, Wearables, Big Data and High Performance Computing (HPC), new families of applications will soon show significant interest in exploiting the capabilities offered by customized heterogeneous hardware such as FPGA, ASIP, MPSoC, heterogeneous CPU+GPU chips and heterogeneous multi-processor clusters. Thus there is an urgent need to design more flexible software abstractions and improved system architectures to fully exploit the benefits of these heterogeneous platforms.

Moreover, heterogeneity shows benefits in various areas. Heterogeneous parallel architectures have the potential to be applied to any sizable workload. Adopting heterogeneous systems to run HPC as well as non-HPC workloads has the potential to deliver higher performance on extreme-scale applications, which is particularly useful when homogeneous servers are too slow. As the HPC community is heading toward the era of exascale machines, these are expected to exhibit an unprecedented level of complexity and size.

Challenge

Analyzing the market, we have found the importance of exploiting parallelism is of increasing significance, as parallelization has become a dominant method of delivering higher performance and improved energy efficiency.
In this context, some of the biggest challenges to future application performance are:

- Future application performance lie with not only efficient node-level execution but power consumption as well,
- Developers need to fully understand, and use an approach that abstracts, the nuances of different hardware configurations and software systems (both rapidly evolving),
- Developers need ways to address additional difficulties in performance, security mixed-criticality and power consumption resulting from the heterogeneous system.
- An important step in software design for low power is that software must correctly fitted to the capabilities of the underlying (and heterogeneous) hardware.

Therefore:

- Because the impact of heterogeneity on all computing tasks is rapidly increasing, innovative architectures, algorithms, and specialized programming environments and tools are needed to efficiently use these new and mixed/diversified parallel architectures.
- A key element of the value chain is the need for software and the underlying programming methodologies that take also into account energy, performance and other requirements of the software applications which run on hardware units.

**Solution**

TANGO approach states that the energy requirements of the software applications which run on hardware units must be incorporated into the overall development and deployment process. Therefore, TANGO will address the total characterization of software with respect to the impact of software structure on power consumption and other dimensions.

Determining the relationship between software structure and its power usage will allow the definition of a set of software power metrics similar in concept to those for hardware. By associating those metrics with software components and libraries it will be possible to not only populate a software development environment with information to predict and illustrate the power requirements of applications enabling the programmer to see the consequences of their work, but also to automatically optimize the code by allowing alternative selections of software components to be made, using power consumption as an additional selection criterion.

In TANGO’s approach, software requirements will not only seek energy optimization, but other different optimizations areas (energy efficiency, performance, data movement and location, cost, time-criticality, security, dependability on target architectures).

**Expected impact**

TANGO will impact on both the IT industry and market; and the research community advancing future application development processes to a new stage in which the development process for parallel architectures will be simplified; will be abstracted from underlying architectures and hardware; and will enable tools to consider optimized control and self-adaptation thanks to various dimensions such as energy efficiency, performance, data movement and location, cost, time-criticality, security, dependability on target architectures.

The key novelty of the project is a reference architecture and its implementation that will include the results of the research work into different optimizations areas (energy efficiency, performance, data movement and location, cost, time-criticality, security, dependability on target architectures).

Moreover, TANGO will include a programming model with built-in support for various hardware architectures including heterogeneous clusters, heterogeneous chips and programmable logic devices. TANGO will create a new cross-layer programming approach for heterogeneous parallel hardware architectures featuring automatic code generation including software and hardware modeling.

Moreover, TANGO will provide mechanisms that allow control of the heterogeneous parallel infrastructures. The most important outcomes of the project will be released as Open Source.

TANGO considers the foundation of a Research Alliance in which it will seek complementary efforts of other research projects, initiatives and IT community organizations to nurture a strong research collaboration, integration and effective promotion of the results.